AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) An apparatus, comprising:

a communication path to exchange information packets;

a processor to process information packets; ~~and~~

a buffer pool cache local to the processor to store free buffer handles for information packets if the buffer pool cache local to the processor is not full; and

a non-local memory to store the free buffer handles for information packets if the buffer pool cache local to the processor is full.

2. (Original) The apparatus of claim 1, wherein the processor and buffer pool cache are formed on the same integrated circuit die.

3. (Original) The apparatus of claim 1, wherein the communication path comprises:

an input path for receiving information packets; and

an output path for transmitting information packets.

4. (Original) The apparatus of claim 1, wherein the communication path comprises:

a memory path for fetching and freeing buffers.

5. (Original) The apparatus of claim 1, wherein the processor comprises:

a receive processor connected to the communication path to process information packets; and

a transmit processor connected to the receive processor and the communication path to process information packets

6. (Original) The apparatus of claim 1, wherein the processor comprises:

a secondary processor connected to the communication path and the buffer pool cache.

7. (Original) The apparatus of claim 1, wherein the communication path connects to at least one of a dynamic random access memory and a static random access memory.

8. (Original) The apparatus of claim 1, wherein the buffer pool cache is a set of next neighbor registers configured to form a next neighbor ring.

9. (Currently amended) The apparatus of claim 1, further comprising:

a communication interface device coupled to the communication path.

10. (Currently amended) A method, comprising:

receiving an information packet; ~~and~~

fetching from a local buffer pool cache a buffer handle to be associated with the information packet if the local buffer pool is non-empty; and

fetching the buffer handle from a non-local memory if the local buffer pool cache is empty.

11. (Original) The method of claim 10, further comprising:

storing the information packet in a buffer associated with the fetched buffer handle.

12. (Original) The method of claim 11, further comprising:

processing the information packet;

transmitting the information packet; and

freeing the buffer handle to the local buffer pool cache.

13. (Cancelled)

14. (Original) The method of claim 12, further comprising:

freeing the buffer handle to a non-local memory when the local buffer pool cache is full.

15. (Original) The method of claim 12, wherein the local buffer pool cache is a set of next neighbor registers configured to form a next neighbor ring.

16. (Original) The method of claim 12, wherein the information packet is processed by at least one of a receive processor, a transmit processor, and a secondary processor.

17. (Currently amended) An apparatus, comprising:

a storage medium having stored thereon instructions that when executed by a machine result in the following:

receiving an information packet; ~~and~~

fetching from a local buffer pool cache a buffer handle to be associated with the information packet if the local buffer pool is non-empty; and

fetching the buffer handle from a non-local memory if the local buffer pool cache is empty.

18. (Original) The apparatus of claim 17, wherein execution of the instructions further results in:

storing the information packet in a buffer associated with the fetched buffer handle.

19. (Original) The apparatus of claim 18, wherein execution of the instructions further results in:

processing the information packet;

transmitting the information packet; and

freeing the buffer handle to the local buffer pool cache.

20. (Currently amended) A system, comprising:

a network processor, including:

a communication path to exchange information packets,

a processor to process information packets;~~, and~~

a buffer pool cache local to the processor to store free buffer handles for information packets when the buffer pool cache to the processor is not full; and

a non-local memory to store the free buffer handles for information packets if the buffer pool cache local to the processor is full; and

an asynchronous transfer mode interface.

21. (Original) The apparatus of claim 20, wherein the processor and buffer pool cache are formed on the same integrated circuit die.